What is claimed is:

1. A spectrum analyzer, comprising:

an input adapted to receive an input signal;

a mixer, coupled to the input, the mixer adapted to produce a down converted signal from the input signal;

an adjustable decimation circuit, coupled to the mixer, that selectively decimates the down converted signal;

a decoder, coupled to the adjustable decimation circuit, that measures power in the decimated signal; and

a control circuit, coupled to the mixer, that selectively controls the frequency of the down converted signals from the mixer to measure power over a frequency spectrum of the input signal.

2. The spectrum analyzer of claim 1, and further including a memory, coupled to the decoder, that stores values related to the measured power.

3. The spectrum analyzer of claim 1, and further including a numerically controlled oscillator, coupled to the mixer and to the control circuit, wherein the control circuit steps the numerically controlled oscillator through a plurality of frequencies.

4. The spectrum analyzer of claim 1, wherein the adjustable decimation circuit includes:

a first stage, responsive to signals from the control circuit, the first stage selectively reducing the sampling rate of the down converted signal based on a characteristic of the input signal; and

a second stage, responsive to signals from the control circuit, the second stage selectively reducing the bandwidth of the down converted signal.

5. The spectrum analyzer of claim 1, wherein the decoder measures the power by calculating a value based on I and Q components of the signal.

6. The spectrum analyzer of claim 5, wherein the decoder calculates the value based on the equation:

$$Power = \sqrt{I^2 + Q^2}$$

7. The spectrum analyzer of claim 3, wherein the control circuit establishes an initial control value, a number of steps and a step size for the control value provided to the numerically controlled oscillator.

8. The spectrum analyzer of claim 3, wherein the control circuit establishes a control value to select a frequency band in a zero span mode.

9. The spectrum analyzer of claim 1, wherein the decoder circuit further includes a log function that calculates a log of the measured power.

10. A method for measuring power of an input signal over a selected frequency spectrum, the method comprising:

mixing the input signal to produce a down converted signal at a selected frequency;

decimating the down converted signal;

measuring a power level of the decimated signal; and

repeating the process of mixing, decimating, measuring and storing to produce power measurements at a plurality of frequencies.

11. The method of claim 10, and further including storing the value for each of the measured power levels.

12. The method of claim 11, and further including reading out and displaying the measured power levels.

13. The method of claim 10, wherein mixing the signal comprises mixing the signal under the control of a numerically controlled oscillator.

14. The method of claim 10, wherein measuring the power level comprises calculating a value based on I and Q components of the signal.

15. The method of claim 14, wherein calculating a value comprises calculating a value for the power level based on the equation:

$$Power = \sqrt{I^2 + Q^2}$$

16. The method of claim 14, wherein calculating a value based on I and Q components of the signal further comprises calculating a log of the measured power level.

17. A method for measuring power of an input signal at a selected frequency, the method comprising:

mixing the input signal to produce a down converted signal at the selected frequency;

decimating the down converted signal;

repeatedly measuring a power level of the decimated signal; and

monitoring the measured power levels over a period of time.

18. The method of claim 17, and further including storing the value for each of the measured power levels.

19. The method of claim 18, and further including reading out and displaying the measured power levels.

20. The method of claim 17, wherein mixing the signal comprises mixing the signal under the control of a numerically controlled oscillator.

21. The method of claim 17, wherein measuring the power level comprises calculating a value based on I and Q components of the signal.

22. The method of claim 21, wherein calculating a value comprises calculating a value for the power level based on the equation:

$$Power = \sqrt{I^2 + Q^2}$$

23. The method of claim 21, wherein calculating a value based on I and Q components of the signal further comprises calculating a log of the measured power level.

24. An analysis system, comprising:

an input adapted to receive an input signal;

a mixer, coupled to the input, the mixer adapted to produce a down converted signal from the input signal;

a numerically controlled oscillator, coupled to the mixer, to provide a signal for down converting the input signal;

an adjustable decimation circuit, coupled to the mixer, that selectively decimates the down converted signal;

a decoder, coupled to the adjustable decimation circuit, that measures power in the decimated signal;

a memory, coupled to the decoder, that stores values related to the measured power; and

a control circuit, coupled to the numerically controlled oscillator and responsive to a processor, that selectively controls the frequency of the down converted signals from the mixer to measure power over a frequency spectrum of the input signal based on values supplied by the processor.

25. The spectrum analyzer of claim 24, wherein the adjustable decimation circuit includes:

a first stage, responsive to signals from the control circuit, the first stage selectively reducing the sampling rate of the down converted signal based on a characteristic of the input signal; and

a second stage, responsive to signals from the control circuit, the second stage selectively reducing the bandwidth of the down converted signal.

26. The spectrum analyzer of claim 24, wherein the decoder measures the power by calculating a value based on I and Q components of the signal.

27. The spectrum analyzer of claim 26, wherein the decoder calculates the value based on the equation:

$$Power = \sqrt{I^2 + Q^2}$$

28. The spectrum analyzer of claim 24, wherein the control circuit establishes an initial control value, a number of steps and a step size for the control value provided to the numerically controlled oscillator.

29. The spectrum analyzer of claim 24, wherein the decoder circuit further includes a log function that calculates a log of the measured power.

30. A digital down conversion circuit with a spectrum analyzer, the circuit comprising:

a plurality of inputs, each input adapted to be coupled to a coaxial cable;

a plurality of down conversion channels, selectably coupled to the plurality of inputs, each down conversion channel programmable to down convert signals at a selected frequency from a selected one of the plurality of inputs; and

a spectrum analyzer, selectably coupled to the plurality of inputs, the spectrum analyzer adapted to measure power levels over a frequency spectrum for a selected one of the plurality of inputs, the spectrum analyzer including:

an input adapted to receive an input signal,

a mixer, coupled to the input, the mixer adapted to produce a down converted signal from the input signal,

an adjustable decimation circuit, coupled to the mixer, that selectively decimates the down converted signal,

a decoder, coupled to the adjustable decimation circuit, that measures power in the decimated signal, and

a control circuit, coupled to the mixer, that selectively controls the frequency of the down converted signals from the mixer to measure power over a frequency spectrum of the input signal.

31. The circuit of claim 30, and further including a memory, coupled to the decoder, that stores values related to the measured power.

32. The circuit of claim 30, and further including a numerically controlled oscillator, coupled to the mixer and to the control circuit, wherein the control circuit steps the numerically controlled oscillator through the plurality of frequencies.

33. The circuit of claim 30, wherein the adjustable decimation circuit includes:

a first stage, responsive to signals from the control circuit, the first stage selectively reducing the sampling rate of the down converted signal based on a characteristic of the input signal; and

a second stage, responsive to signals from the control circuit, the second stage selectively reducing the bandwidth of the down converted signal.

34. The circuit of claim 30, wherein the decoder measures the power by calculating a value based on I and Q components of the signal.

35. The circuit of claim 34, wherein the decoder calculates the value based on the equation:

$$Power = \sqrt{I^2 + Q^2}$$

36. The circuit of claim 32, wherein the control circuit comprises a control circuit that establishes an initial control value, a number of steps and a step size for the control value provided to the numerically controlled oscillator.

37. The circuit of claim 30, wherein the decoder circuit further includes a log function that calculates a log of the measured power.

38. The circuit of claim 30, wherein a plurality of down conversion channels, selectably coupled to the plurality of inputs comprises a plurality of down conversion channels, multiplexed to the plurality of inputs wherein selectably coupled.

39. A digital down conversion circuit with a signal analyzer, the circuit comprising:

a plurality of inputs, each input adapted to be coupled to a coaxial cable;

a plurality of down conversion channels, selectably coupled to the plurality of inputs, each down conversion channel programmable to down convert signals at a selected frequency from a selected one of the plurality of inputs; and

a signal analyzer, selectably coupled to the plurality of inputs, the signal analyzer selectively providing at least one of frequency domain and time domain analysis of selected signals from the plurality of inputs.

40. An analysis system, comprising:

an input adapted to receive an input signal;

a mixer, coupled to the input, the mixer adapted to produce a down converted signal from the input signal;

a numerically controlled oscillator, coupled to the mixer, to provide a signal for down converting the input signal;

an adjustable decimation circuit, coupled to the mixer, that selectively decimates the down converted signal;

a decoder, coupled to the adjustable decimation circuit, that measures power in the decimated signal;

a memory, coupled to the decoder, that stores values related to the measured power; and

a control circuit, coupled to the numerically controlled oscillator and responsive to a processor, that selectively controls the frequency of the down converted signals from the mixer to measure power for at least one frequency range of the input signal based on values supplied by the processor.

41. The analysis system of claim 40, wherein the control circuit selectively generates control signals for the numerically controlled oscillator that step the numerically controlled oscillator through a plurality of frequencies.

42. The analysis system of claim 40, wherein the control circuit selectively generates a control signal for the numerically controlled oscillator to establish a frequency for time domain analysis.

43. The analysis system of claim 40, wherein the control circuit selects between stepping the numerically controlled oscillator through a plurality of frequencies and establishing a frequency for time domain analysis.

44. A signal analyzer, comprising:

an input adapted to receive an input signal;

a mixer, coupled to the input, the mixer adapted to produce a down converted signal from the input signal;

an adjustable decimation circuit, coupled to the mixer, that selectively decimates the down converted signal;

a threshold comparator, coupled to the adjustable decimation circuit, that compares the decimated signal with a selected threshold over a period of time; and

a control circuit, coupled to the mixer, that selectively controls the frequency of the down converted signals from the mixer to select a frequency of the input signal for time domain analysis.

45. The signal analyzer of claim 44, and further including a numerically controlled oscillator, coupled to the mixer and to the control circuit, wherein the control circuit selects a frequency for the numerically controlled oscillator.

46. The signal analyzer of claim 44, wherein the adjustable decimation circuit includes:

a first stage, responsive to signals from the control circuit, the first stage selectively reducing the sampling rate of the down converted signal based on a characteristic of the input signal; and

a second stage, responsive to signals from the control circuit, the second stage selectively reducing the bandwidth of the down converted signal.

47. The signal analyzer of claim 44, wherein the threshold comparator calculates a value based on I and Q components of the signal to compare with the threshold.

48. The signal analyzer of claim 44, wherein the decoder calculates the value based on the equation:

$$Value = |I| + |Q|$$

49. The signal analyzer of claim 44, wherein the threshold of the threshold comparator is selected based on expected power level and modulation technique.

50. The signal analyzer of claim 44, wherein the threshold comparator compares the decimated signal with the selected threshold over a symbol period.

51. A method for monitoring noise levels of an input signal at a selected frequency, the method comprising:

mixing the input signal to produce a down converted signal at the selected frequency;

decimating the down converted signal;

computing a value based on the decimated signal;

comparing the value with a threshold; and

monitoring the comparisons to provide time domain analysis of the signal.

52. The method of claim 51, wherein monitoring the comparisons comprises monitoring the comparisons to determine an estimate of the noise in the input signal.

53. The method of claim 51, wherein computing a value comprises computing a value according to the equation:

$$Value = |I| + |Q|$$

wherein I and Q comprise the in-phase and quadrature-phase components of the input signal.

54. The method of claim 51, wherein mixing the signal comprises mixing the signal under the control of a numerically controlled oscillator.

55. The method of claim 51, wherein computing a value based on the decimated signal comprises computing a value over a symbol period.

56. The method of claim 51, wherein monitoring the comparisons comprises tracking the number of times the computed value exceeds the threshold.

57. The method of claim 51, wherein comparing the value with the threshold comprises comparing the value with the threshold established based on one half of the distance between adjacent points in a constellation for a selected modulation.